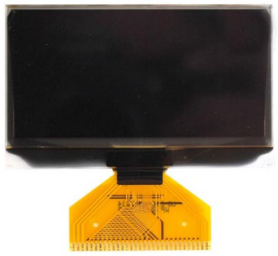
OLD-030015-00

2.42-inch Green OLED Display

128 × 64 pixels / Passive matrix / SSD1305 controller

A compact monochrome display with a 55.01 × 27.49 mm active area, 1/64 drive duty, and selectable serial or parallel host interfaces.



KEY PARAMETER	SPECIFICATION
Panel dimensions	60.50 × 37.00 × 2.00 mm
Active area	55.01 × 27.49 mm (2.42-inch nominal diagonal)
Resolution / pixel pitch	128 × 64 / 0.43 × 0.43 mm
Pixel size / weight	0.40 × 0.40 mm / 8.81 g
Full-brightness luminance	100 cd/m² minimum; 120 cd/m² typical
Fully dimmed luminance	0.20 cd/m² target; 0.30 cd/m² maximum — both unconfirmed. Lowest achievable luminance: TBD; measurement required.
Contrast / viewing angle	>2000:1 / >160°
Logic / panel supply (typical)	VDD 2.8 V / VCC 13 V
Interfaces	4-wire SPI, I²C, 8-bit 68XX and 8-bit 80XX parallel
Operating temperature	-40 to +70 °C
FPD.DEV part number	OLD-030015-00

Optical values: VDD = 2.8 V and VCC = 13 V, using the initialization on page 14. See pages 6-8 for limits and conditions.

Engineering information

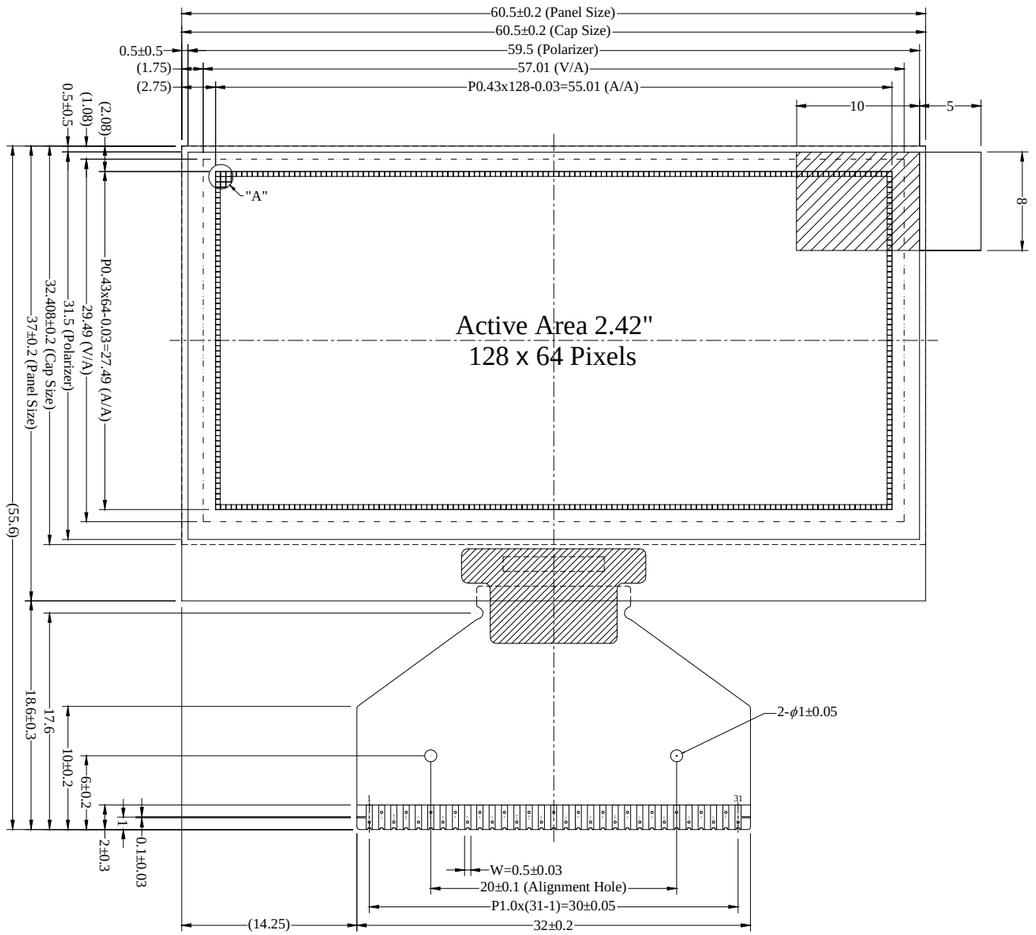
Mechanical drawing 2 • Pinout 3-4 • Circuit 5 • Ratings and optical data 6 • Chromaticity charts 7 • DC characteristics 8 • Timing 9-12 • Power and reset 13 • Initialization 14 • Reliability and inspection 15-18 • Handling and design 19-20

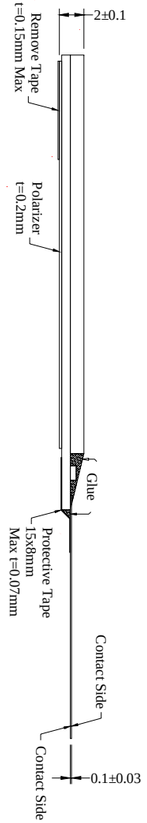
Preliminary technical data for engineering review. FPD.DEV part number OLD-030015-00; engineering release remains pending. Reliability data are supplied specifications, not evidence of FPD.DEV qualification. NVIS compliance is not established by this datasheet.

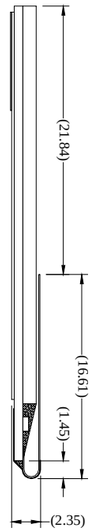
The Future of Display and Systems Development.

Mechanical outline - no touch panel

Dimensions in millimeters. Explicit dimensional tolerances are retained. Do not scale this drawing. Connector contact sides and pin numbering are shown in the views.

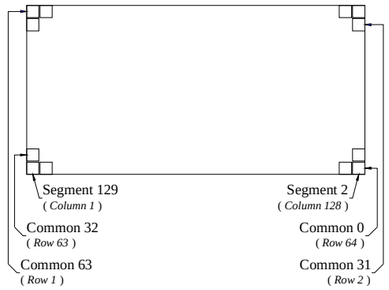


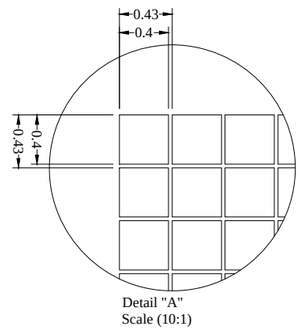




Unless Otherwise S cifi	
Unit	m
General Roughness	
To rance	
Dimension	±0 30
Ang e	±1

General tolerance block as supplied. Partly illegible; confirm before manufacture.





Detail "A"
Scale (10:1)

Pin	Symbol
1	N.C. (GND)
2	VCC
3	VCOMH
4	IREF
5	D7
6	D6
7	D5
8	D4
9	D3
10	D2
11	D1
12	D0
13	E/RD#
14	R/W#
15	D/C#
16	RES#
17	CS#
18	NC
19	BS2
20	BS1
21	VDD
22	N.C.
23	N.C.
24	N.C.
25	N.C.
26	N.C.
27	N.C.
28	N.C.
29	N.C.
30	VSS
31	N.C. (GND)

Panel: 60.50 × 37.00 × 2.00 mm | Active area: 55.01 × 27.49 mm | Drawing references: nominal 2.42-inch diagonal; 128 × 64 pixels.

Pin assignment

Use the contact-side orientation in the mechanical drawing. Signal names and pin numbers below describe the 31-position display interface. # indicates an active-low signal.

PIN	SIGNAL	I/O	FUNCTION
1	N.C. (GND)	-	Supporting pin; connect to external ground
2	VCC	I/O	External OLED panel supply
3	VCOMH	I/O	COM high-level voltage; capacitor to VSS
4	IREF	I	Current reference; resistor to VSS; below 10 µA
5	D7	I/O	Parallel data bit 7
6	D6	I/O	Parallel data bit 6
7	D5	I/O	Parallel data bit 5
8	D4	I/O	Parallel data bit 4
9	D3	I/O	Parallel data bit 3
10	D2	I/O	Parallel bit 2; I²C SDAOUT
11	D1	I/O	Parallel bit 1; SPI SDIN; I²C SDAIN
12	D0	I/O	Parallel bit 0; SPI SCLK; I²C SCL
13	E/RD#	I	68XX enable / 80XX read
14	R/W#	I	68XX read/write / 80XX write
15	D/C#	I	Data/command selection; I²C SA0
16	RES#	I	Reset input, active low
17	CS#	I	Chip select, active low
18	N.C.	-	Reserved
19	BS2	I	Interface selection
20	BS1	I	Interface selection
21	VDD	I	External logic supply
22-29	N.C.	-	Reserved
30	VSS	I	Ground and voltage reference
31	N.C. (GND)	-	Supporting pin; connect to external ground

Interface selection and signal functions

INTERFACE	BS1 (PIN 20)	BS2 (PIN 19)
I²C	1	0
4-wire SPI	0	0
8-bit 68XX parallel	0	1
8-bit 80XX parallel	1	1

Data and command control

D/C# high selects display data; low selects the command register. In serial mode the same selection applies to SDIN. In I²C mode D/C# serves as SA0 for slave-address selection.

68XX parallel interface

E/RD# is the enable input E. Read/write operation starts when E is high and CS# is low. R/W# high selects a read; R/W# low selects a write.

80XX parallel interface

E/RD# is the active-low read input RD#. A read starts when RD# and CS# are low. R/W# becomes the active-low write input WR#; a write starts when WR# and CS# are low.

Serial and I²C connections

In SPI mode D1 is serial data input SDIN and D0 is serial clock SCLK. In I²C mode connect D2 and D1 together as SDAOUT and SDAIN; D0 is SCL.

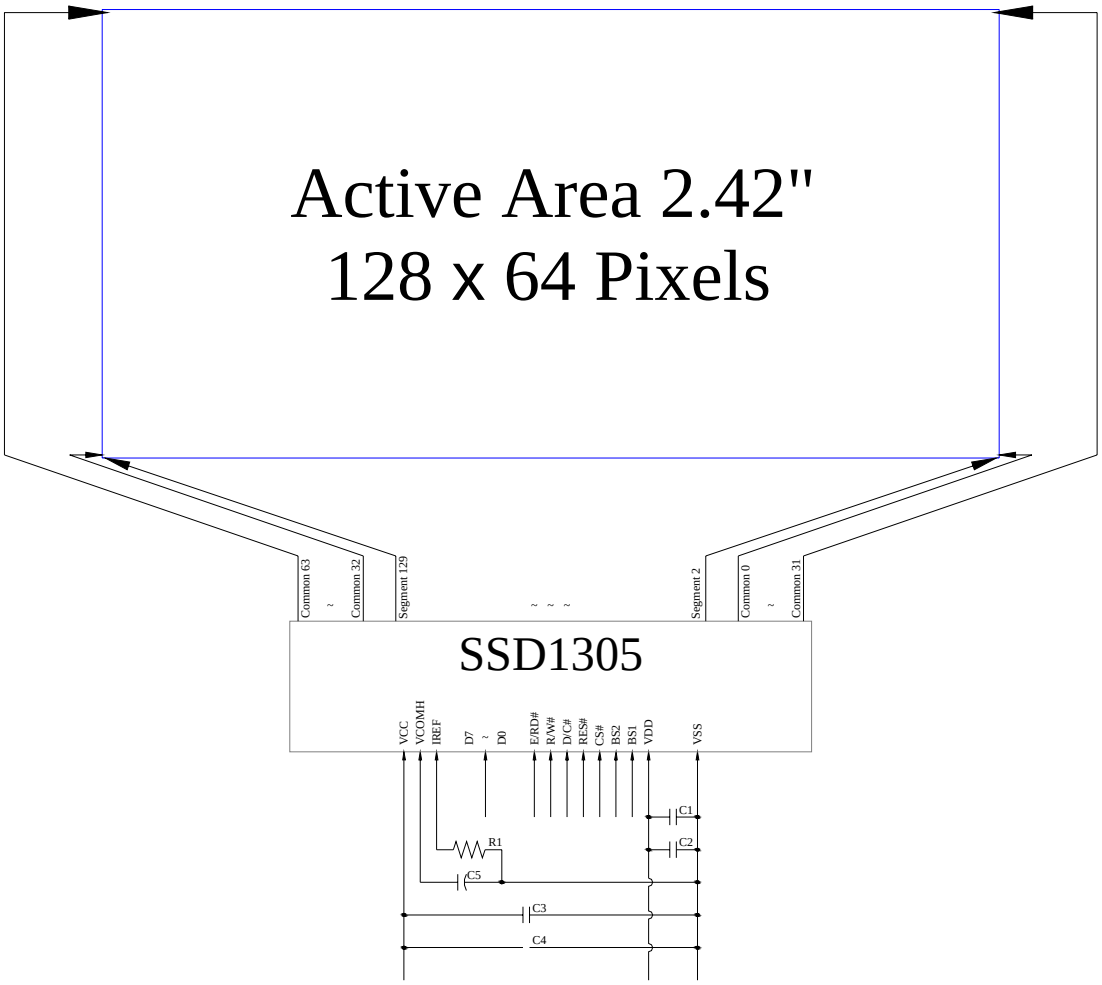
Reset and chip select

RES# low initializes the controller and driver. The controller accepts MCU communication when CS# is low.

Supply, reference and reserved pins

Connect VDD and VCC to their external supplies and VSS to external ground. Connect a resistor from IREF to VSS and keep reference current below 10 µA. Connect a capacitor from VCOMH to VSS. Supporting pins 1 and 31 must connect to external ground; the remaining N.C. pins are reserved.

Block diagram and external components



REFERENCE	VALUE / CONNECTION
C1, C3	0.1 µF
C2	4.7 µF
C4	10 µF
C5	4.7 µF / 25 V tantalum capacitor
R1	910 kΩ; R1 = (voltage at IREF - BGGND) / IREF
Interface selection	BS1 and BS2
MCU interface signals	D7-D0, E/RD#, R/W#, D/C#, RES# and CS#

Panel: 128 × 64; controller reset: 132 × 64. See segment mapping above. Controller reference: Solomon Systech SSD1305 Rev 1.8 (July 2007) — 132 × 64 OLED/PLED driver IC. Use this panel datasheet for the 31-pin module connections.

Ratings, chromaticity and NVIS filtering

ABSOLUTE MAXIMUM	SYMBOL	MIN	MAX	UNIT
Logic supply	VDD	-0.3	4	V
Display supply	VCC	0	15	V
Operating temperature	TOP	-40	70	°C
Storage temperature	TSTG	-40	85	°C

Voltages reference VSS = 0 V. Absolute maxima are stress limits; exceeding them can cause permanent damage. Normal operating conditions are on page 8.

Optical characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Full-brightness luminance	100	120	-	cd/m²
Fully dimmed luminance*	TBD	0.20 target	0.30	cd/m²
CIE 1931 green x	0.27	0.31	0.35	-
CIE 1931 green y	0.58	0.62	0.66	-
Dark-room contrast	>2000:1	-	-	-
Viewing angle	>160	-	-	degrees

* Fully dimmed target and maximum are unconfirmed design values. Lowest achievable luminance at the minimum brightness setting: TBD — measurement required.

Optical measurements: VDD = 2.8 V; VCC = 13 V; initialization on page 14. Luminance and VCC depend on panel characteristics and configuration. Chromaticity limits are CIE 1931 x/y.

Estimated operating life

40,000 hours minimum listed at 120 cd/m². VCC = 13 V, 25 °C, 50% checkerboard; initialization on page 14. Endpoint: 50% of initial luminance. Estimated from accelerated high-temperature operation; supplied characterization, not an FPD.DEV service-life guarantee.

NVIS filtering requirements

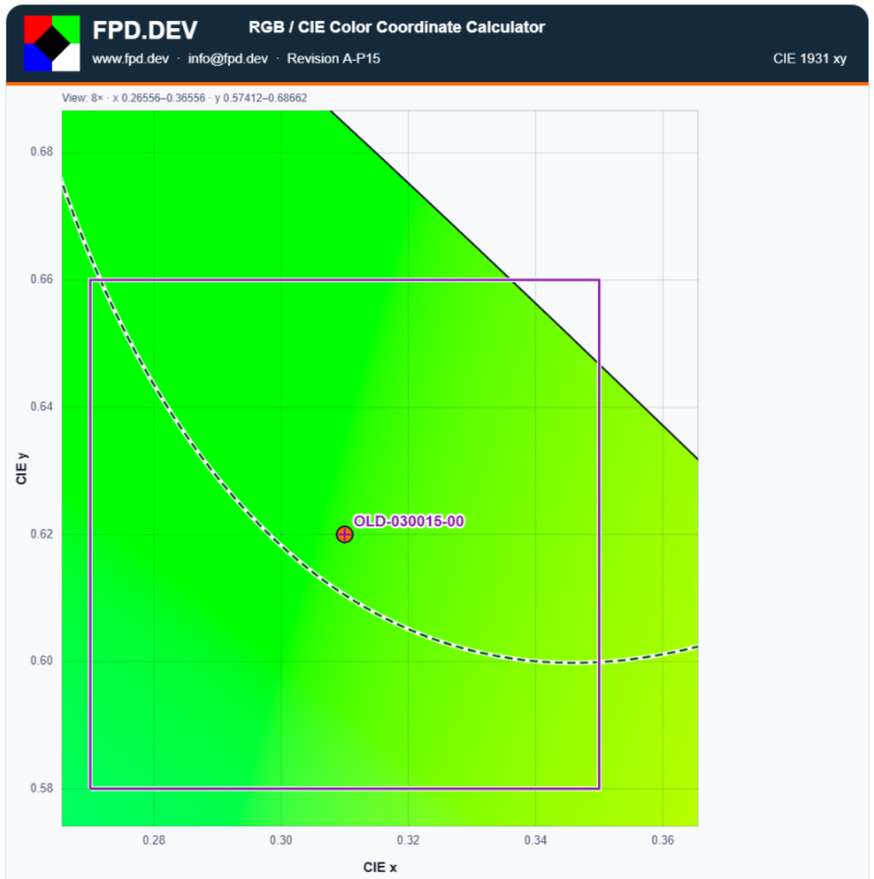
An additional optical filter is required to bring the full display chromaticity range within the MIL-STD-3009 NVIS Green B boundary. Additional filtering may be required to meet NVIS Class B spectral cutoff / radiance requirements.

Verify the filtered display using measured emission and filter-transmission spectra at the specified operating conditions. No NVIS compliance or qualified filter configuration is established here.

The independent x/y limits define a square centered at (0.31000, 0.62000), with total width and height 0.08000. See the paired calculator views on page 7.

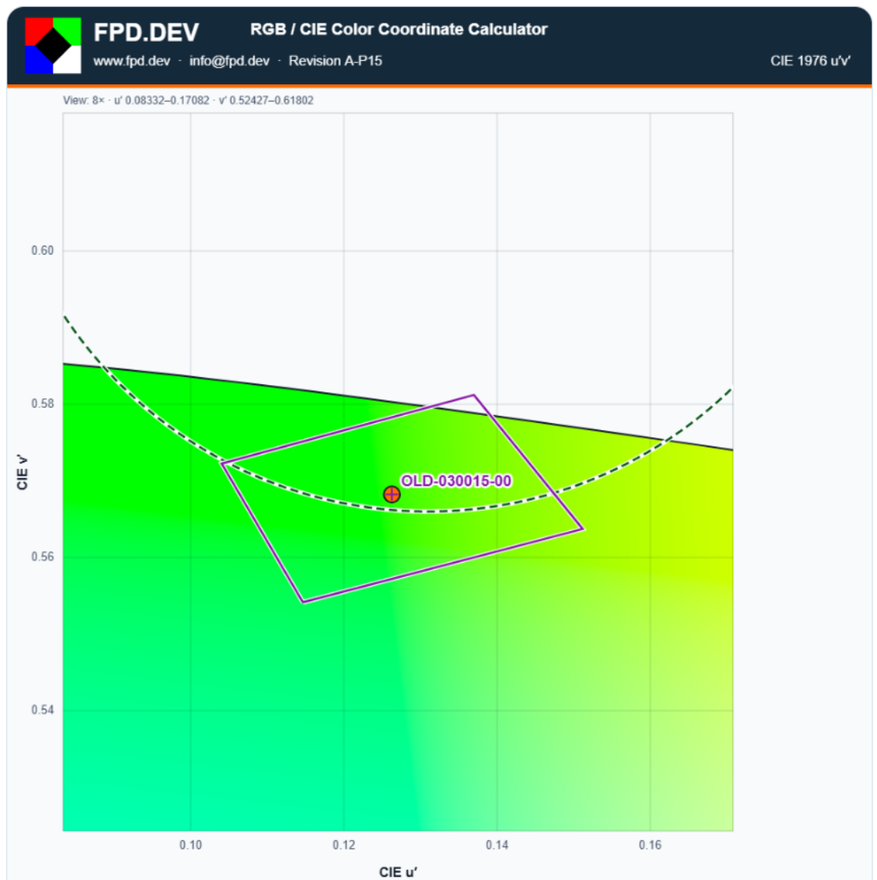
Chromaticity specification in xy and u′v′

CIE 1931 xy: x = 0.31000 ± 0.04000; y = 0.62000 ± 0.04000. The same boundary transforms to a quadrilateral in CIE 1976 u′v′. Dashed boundary: NVIS Green B.



GB: NVIS Green B [u′v′] centroid (0.13100, 0.62300) · circle · r 0.05700
Custom: OLD-030015-00 [xy] centroid (0.31000, 0.62000) · box · width 0.08000 · height 0.08000
Chromaticity-region overlap · target: OLD-030015-00 · area basis CIE 1931 xy
Target area: ≈ 98.6% physically realizable · ≈ 1.4% outside realizable region
Full = complete regions; realizable = spectral locus + line of purples.
NVIS Green B: full T/R 53.5% / 1.4% · realizable T/R 52.8% / 48.0%
MC1 NVIS Green B: xy (0.32344, 0.63345) · clearance 0.02655
MC = approximate maximum-clearance point; distance in target CIE system.
T = target area; R = reference area. Approximate geometry, not compliance.

MIL-STD-3009 Figure 2 / Table II · Circle limits in CIE 1976 u′v′
CIE: cie.co.at/data-tables · Derived data CC BY-SA 4.0 · Geometry only



GB: NVIS Green B [u′v′] centroid (0.13100, 0.62300) · circle · r 0.05700
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MIL-STD-3009 Figure 2 / Table II · Circle limits in CIE 1976 u′v′
CIE: cie.co.at/data-tables · Derived data CC BY-SA 4.0 · Geometry only

DC electrical characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Logic supply	VDD	2.4	2.8	3.5	V
Display supply	VCC	12.5	13	13.5	V
High-level input	VIH	0.8 × VDD	-	VDD	V
Low-level input	VIL	0	-	0.2 × VDD	V
High-level output	VOH	0.9 × VDD	-	VDD	V
Low-level output	VOL	0	-	0.1 × VDD	V
Logic operating current	IDD	-	180	300	µA
Panel current; 50% on	ICC	-	23.0	28.8	mA
Panel current; 100% on	ICC	-	26.5	33.1	mA
Logic sleep current	IDD,SLEEP	-	1	10	µA
Panel sleep current	ICC,SLEEP	-	2	10	µA

Test conditions and notes

• Input/output levels are listed at IOUT = 100 µA and 3.3 MHz.

• Panel-current measurements use VDD = 2.8 V and VCC = 13 V, with 50% or 100% of the display area on as specified.

• The operating and optical data use the initialization sequence on page 14.

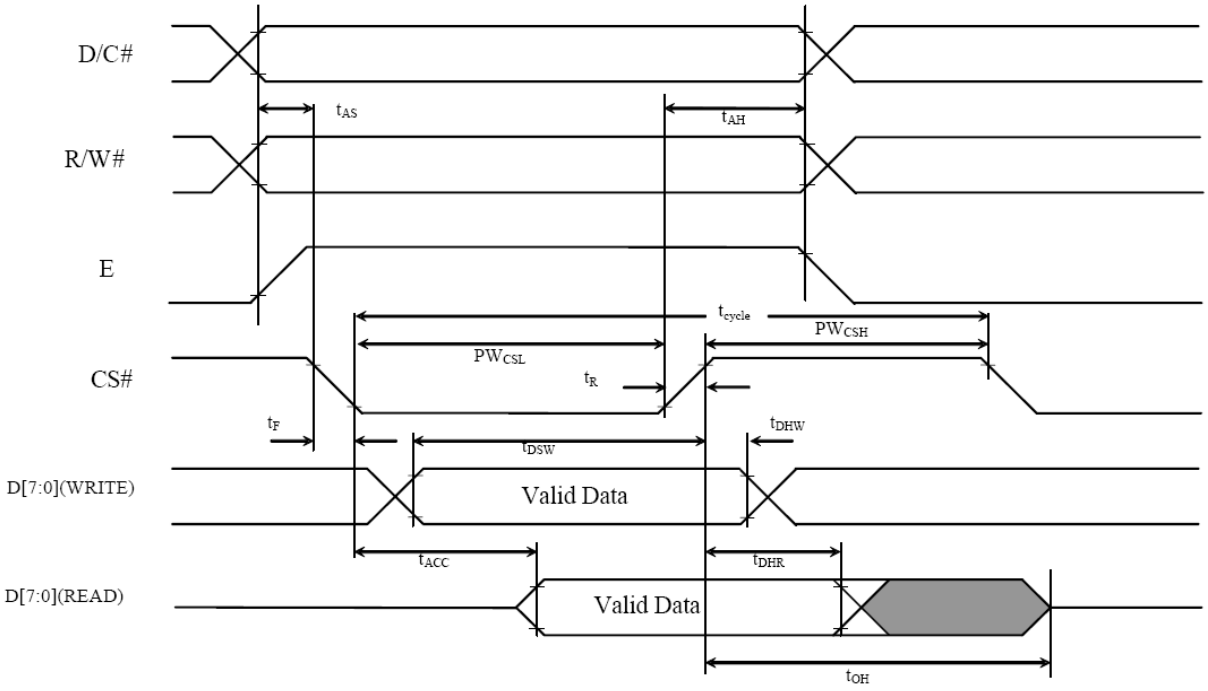
• Display supply and brightness may vary with panel characteristics and the requested configuration.

• The DC table does not specify a guaranteed dimming floor, chromaticity at low luminance, or NVIS spectral performance.

68XX parallel interface timing

Timing conditions: VDD - VSS = 2.4 to 3.5 V; ambient temperature 25 °C.

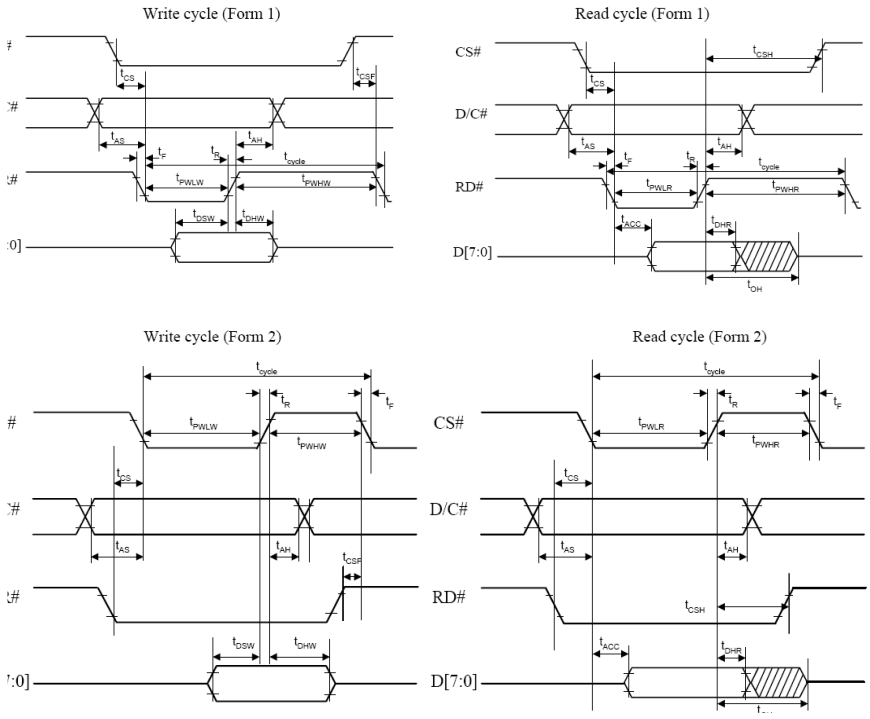
SYMBOL	DESCRIPTION	MIN	MAX	UNIT
tcycle	System cycle time	300	-	ns
tAS	Address setup time	0	-	ns
tAH	Address hold time	0	-	ns
tDSW	Write data setup time	40	-	ns
tDHW	Write data hold time	7	-	ns
tDHR	Read data hold time	20	-	ns
tOH	Output disable time	-	70	ns
tACC	Access time	-	140	ns
PWCSL	CS low pulse width, read / write	120 / 60	-	ns
PWCSH	CS high pulse width, read / write	60 / 60	-	ns
tR / tF	Rise / fall time	-	15 / 15	ns



80XX parallel interface timing

Timing conditions: VDD - VSS = 2.4 to 3.5 V; ambient temperature 25 °C.

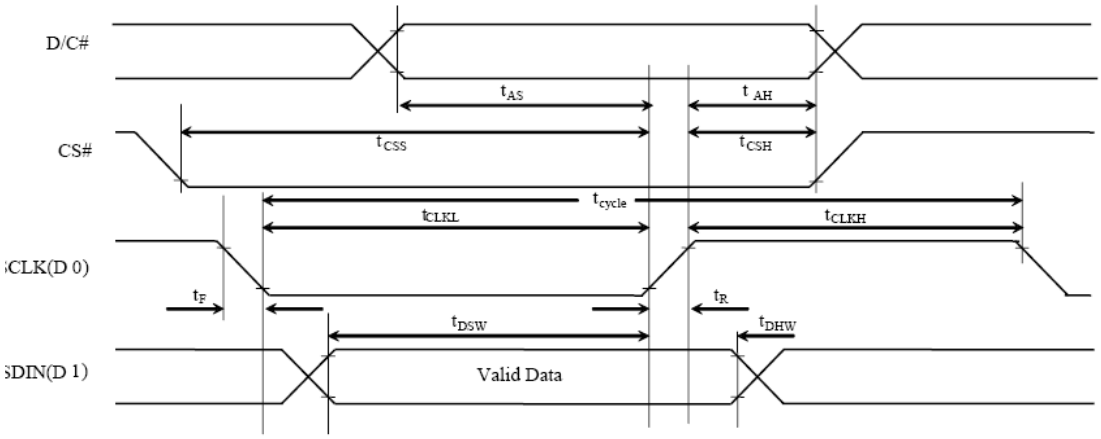
SYMBOL	DESCRIPTION	MIN	MAX	UNIT
tcycle	Clock cycle time	300	-	ns
tAS / tAH	Address setup / hold time	10 / 0	-	ns
tDSW / tDHW	Write data setup / hold time	40 / 7	-	ns
tDHR	Read data hold time	20	-	ns
tOH / tACC	Output disable / access time	-	70 / 140	ns
tPWLR	Read low time	120	-	ns
tPWLW	Write low time	60	-	ns
tPWHR / tPWHW	Read / write high time	60 / 60	-	ns
tCS	Chip-select setup time	0	-	ns
tCSH	Chip-select hold to read signal	0	-	ns
tCSF	Chip-select hold time	20	-	ns
tR / tF	Rise / fall time	-	15 / 15	ns

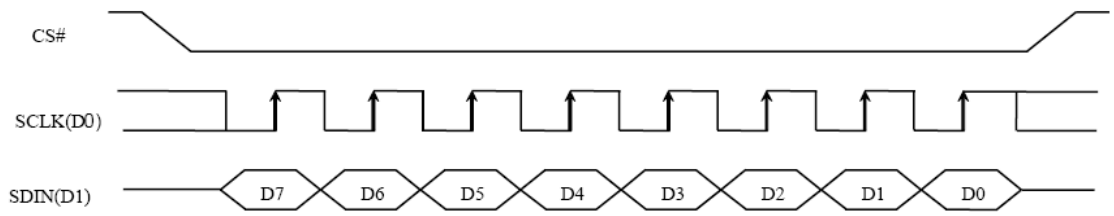


SPI serial interface timing

Timing conditions: VDD - VSS = 2.4 to 3.5 V; ambient temperature 25 °C.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
tcycle	Clock cycle time	250	-	ns
tAS / tAH	Address setup / hold time	150 / 150	-	ns
tCSS	Chip-select setup time	120	-	ns
tCSH	Chip-select hold time	60	-	ns
tDSW	Write data setup time	50	-	ns
tDHW	Write data hold time	15	-	ns
tCLKL	Serial clock low time	100	-	ns
tCLKH	Serial clock high time	100	-	ns
tR / tF	Rise / fall time	-	15 / 15	ns

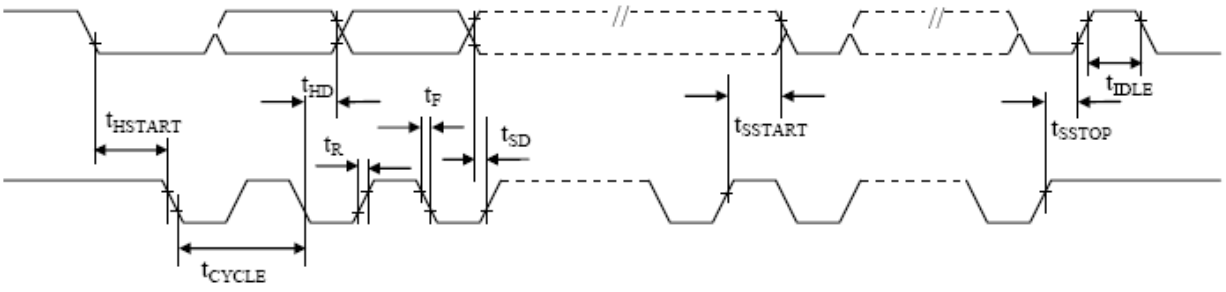




I²C interface timing

Timing conditions: VDD - VSS = 2.4 to 3.5 V; ambient temperature 25 °C.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
tcycle	Clock cycle time	2.5	-	µs
tHSTART	Start-condition hold time	0.6	-	µs
tHD	Data hold time, SDAOUT	0	-	ns
tHD	Data hold time, SDAIN	300	-	ns
tSD	Data setup time	100	-	ns
tSSTART	Repeated-start setup time	0.6	-	µs
tSSTOP	Stop-condition setup time	0.6	-	µs
tR	Data / clock rise time	-	300	ns
tF	Data / clock fall time	-	300	ns
tIDLE	Idle time before new transmission	1.3	-	µs



Separate SDAIN and SDAOUT hold-time requirements are retained. In I²C operation D1 and D2 are connected together, as described on page 4.

Power sequencing and reset

Allow the OLED panel to charge and discharge by sequencing the logic and panel supplies with the specified delays.

POWER UP	POWER DOWN
1. Power up VDD.	1. Send display-off command.
2. Send display-off command.	2. Power down VCC.
3. Initialize the controller.	3. Delay 100 ms after VCC reaches 0 and the panel is fully discharged.
4. Clear the screen.	4. Power down VDD.
5. Power up VCC.	
6. Delay 100 ms after VCC is stable.	
7. Send display-on command.	

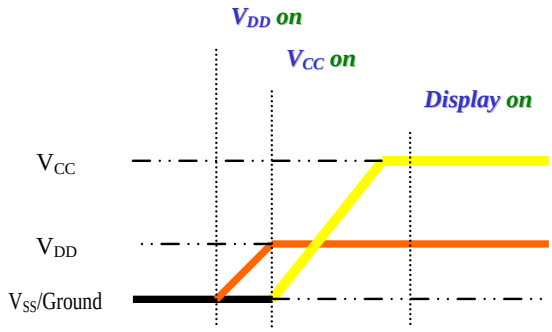
Supply precautions

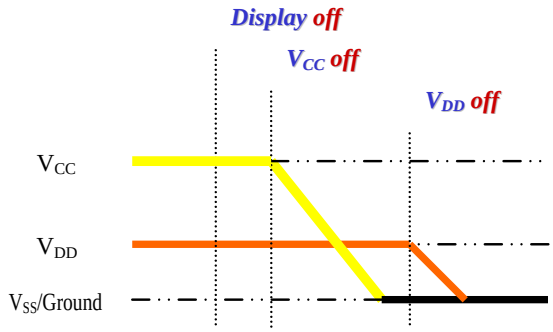
An internal ESD circuit connects VDD and VCC. When VDD is on and VCC is off, VCC becomes lower than VDD. Keep VCC floating (disabled) when off. Do not pull VDD or VCC directly to ground. Do not power down VDD before VCC.

State after RES# is driven low

Display off; 132 × 64 controller mode; normal segment and display-data mapping (SEG0 → column 00h and COM0 → row 00h); serial shift-register data cleared; display start line at RAM address 0; column counter at 0; normal COM scan direction; contrast register at 80h; normal display mode equivalent to A4h.

The controller reset width is distinct from the panel's 128-pixel active width. Consult the SSD1305 technical manual for full command and reset requirements.





Initialization example

Sequence preserved in the order shown by the source flowchart. Coordinate supply switching with page 13; this table is not a substitute for the SSD1305 technical manual.

STEP	FUNCTION	BYTES (HEX)
1	Display off	AE
2	Clock divide / oscillator frequency	D5, A0
3	Multiplex ratio	A8, 3F
4	Display offset	D3, 00
5	Display start line	40
6	Master configuration	AD, 8E
7	Area-color / low-power display mode	D8, 05
8	Segment remap	A1
9	COM output scan direction	C8
10	COM pin hardware configuration	DA, 12
11	Look-up table	91, 3F, 3F, 3F, 3F
12	Bank 0 current control	81, 5F
13	Pre-charge period	D9, 82
14	VCOMH deselect level	DB, 3C
15	Entire display on/off	A4
16	Normal / inverse display	A6
17	Clear screen	Clear display RAM
18	Display on	AF

If noise corrupts the display, reset the module to recover operation. Periodic command and display-data refresh is recommended as part of system-level noise recovery.

Reliability and inspection conditions

RELIABILITY TEST	CONDITIONS
High-temperature operation	70 °C, 240 h
Low-temperature operation	-40 °C, 240 h
High-temperature storage	85 °C, 240 h
Low-temperature storage	-40 °C, 240 h
High-temperature / humidity operation	60 °C, 90% RH, 120 h
Thermal shock	-40 °C ↔ 85 °C; 24 cycles; 60 min dwell

Acceptance criterion: operational functions work. Test samples exclude the polarizer. No moisture condensation is permitted during testing. After testing, allow 2 h at room temperature before checking at 23 ± 5 °C and 55 ± 15% RH. These are supplied test conditions; no FPD.DEV test execution is implied.

Visual-inspection environment

PARAMETER	REQUIREMENT
Temperature / relative humidity	23 ± 5 °C / 55 ± 15% RH
Illumination	30 W fluorescent lamp
Panel-to-lamp distance	≥50 cm
Panel-to-inspector distance	≥30 cm
Handling / work surface	Finger gloves or finger covers; antistatic inspection table or jig

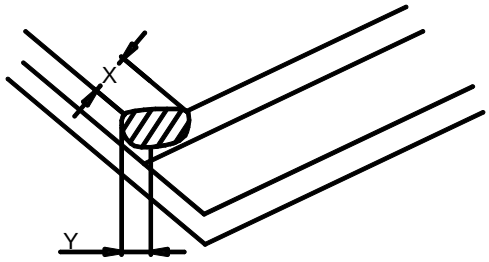
Acceptable quality levels

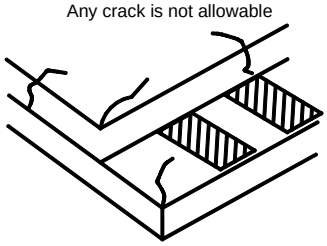
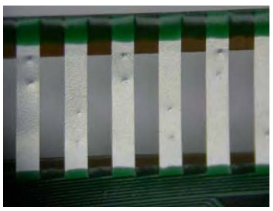
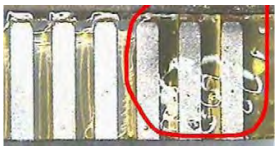
CLASS	AQL	APPLICATION
Major	0.65	Display-on pattern defects
Minor	1.0	Display-off cosmetic defects

A sampling standard, lot-size plan and acceptance/rejection numbers are not specified in the supplied document.

Cosmetic inspection - non-active area

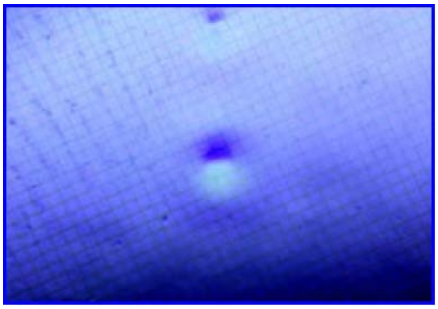
Display off. Dimensions in millimeters. Photographs and drawings illustrate the defect types; they are not images of an inspected delivery lot.

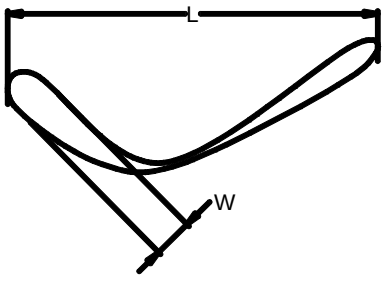
Check Item	Classification	Criteria
Panel General Chipping	Minor	X>6mm (Along with Edge) Y>1mm (Perpendicular to edge) 

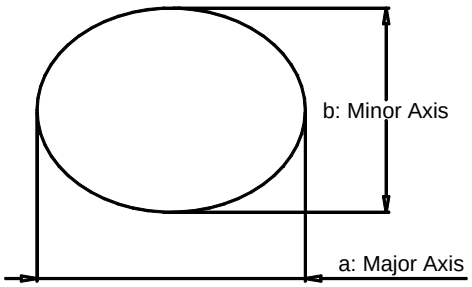
Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Termial Lead Prober Mark	Acceptable	
Glue or Contamination on Pin	Minor	
Ink marking on Back Side of Panel (Exclude on Film)	Acceptable	Ignore for Any

Cosmetic inspection - active area

Perform any necessary exposed-panel inspection in a clean environment (class 10k as specified). Keep the protective film in place during the cosmetic check.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches,Fiber,Line-Shape Defect (On Polarizer)	Minor	W≤0.1 Ignore W>0.1 L≤2 n≤1 L>2 n=0
Dirt, Black Spot, Foreign Material (On Polarizer)	Minor	Φ≤0.1 Ignore 0.1<Φ≤0.25 n≤1 0.25<Φ n=0
Dent,Bubbles,White Spot (Any Transparent Spot on Polarizer)	Minor	Φ≤0.5 Ignore if no Influence on Display 0.5<Φ n=0 
Fingerpint ,Flow Mark (On Polarizer)	Minor	Not Allowable

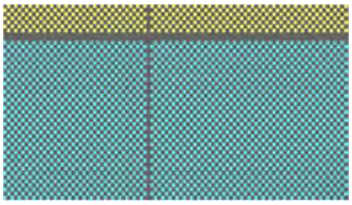
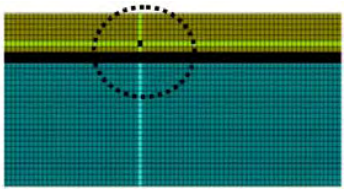
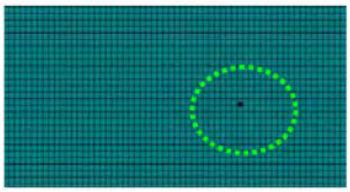
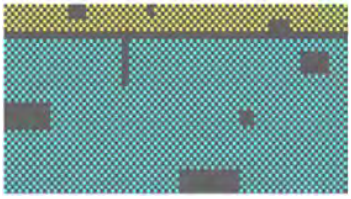
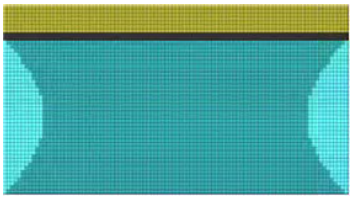




W = defect width; L = defect length; Φ = (a + b) / 2, with a the major axis and b the minor axis. Units: mm. n = allowed defect count.

Display-on pattern inspection

All six listed pattern defects are classified as major (AQL 0.65). Examples are retained for visual identification.

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

Handling and cleaning precautions

Protect the glass and polarizer

The panel is glass. Avoid impacts and drops. If it breaks and internal organic material escapes, do not inhale or ingest the material. Do not press on the display surface or adjacent cell structure. The polarizer is soft and scratches easily.

Clean without solvents

Remove surface contamination using suitable adhesive cleaning tape. Do not breathe on the surface or wipe it with solvent-containing cloth. Ethyl alcohol can cloud the polarizer; water, ketones and aromatic solvents can also damage it.

Support the assembly

Handle the module carefully during installation. Avoid excessive force, stress or pressure. Do not over-bend the film carrying electrode traces. Provide adequate housing rigidity and avoid stress on the driver IC or surrounding molded sections. Do not disassemble or modify the module.

Control electrostatic discharge

Ground personnel and assembly tools, including soldering irons. Avoid dry assembly conditions that promote static buildup. Removing protective film can generate static electricity. Avoid touching pins, electrodes and FPC pattern traces.

Remove protective film before final assembly

Long storage can leave adhesive residue when the film is removed. Remove residue using the compatible adhesive-tape method described above. Retain the film during cosmetic inspection.

Keep the module dry and correctly powered

Do not apply input signals while logic power is off. Do not energize the module when dew or water is present or under high-humidity conditions that can corrode electrodes.

Storage, design and operating precautions

Storage

Keep modules in antistatic bags, preferably in their original protective packaging. Avoid direct sunlight, fluorescent-light exposure, high temperature, high humidity and storage below 0 °C. Prevent droplets and condensation. This handling recommendation is distinct from the absolute storage-temperature rating.

Electrical and mechanical design

Stay within absolute maximum ratings and satisfy VIH/VIL limits. Keep signal cables short and control interference with nearby devices. Provide equipment-level EMI measures. The source recommends overcurrent protection in VDD, with 0.5 A as a suggested value. Fasten the external plastic housing section where provided; verify the mounting arrangement for the delivered module.

Power interruption

Unexpected removal of the main supply while the display is operating bypasses the specified power-down sequence; correct module behavior and quality are not assured under that condition.

Fixed patterns and image retention

Long operation with a fixed pattern may cause an afterimage or slight contrast deviation. The supplied guidance states that recovery may occur after an unused interval; the behavior must be assessed for the intended application.

Shield the exposed driver

Light on the exposed OLED driver can change semiconductor behavior and cause malfunction. Shield the driver from light during use and inspection.

Noise recovery

Excessive noise may alter controller status and display data. Suppress noise in the system design and consider periodic command re-initialization and retransmission of display data.

Disposal

Use qualified waste handlers and comply with applicable environmental and hygiene requirements when disposing of the display module.